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PTO-1449 (Modified)  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA001C14	SERIAL NUMBER 10/028,077
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE December 21, 2001	GROUP ART UNIT 2181

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,761,567	Aug. 2, 1988	Walters, Jr. et al.	307	269	
MA	5,101,117	Mar. 31, 1992	Johnson et al.	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
DA	sho 58-31637A	Feb 24, 1983	Japan	—	—	
MA	sho 59-165285A	Mar. 11, 1983	Japan	—	—	
DA	sho 60-261095A	June 6, 1984	Japan	—	—	
DA	sho 63-300310	Dec. 7, 1988	Japan	—	—	
DA	hei 2-8950	Jan 12, 1990	Japan	—	—	
DA	sho 58-184626A	Oct 28, 1983	Japan	—	—	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)


EXAMINER <i>Glen Anne</i>	DATE CONSIDERED <i>5/14/2002</i>
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BA	4,785,428	Nov. 15, 1988	Bajwa et al.	—	—	
BA	4,658,381	Apr. 14, 1987	Reed et al.	—	—	
BA	4,953,130	Aug. 28, 1990	Houston	—	—	
BA	5,056,064	Oct. 8, 1991	Iwahashi et al.	—	—	
BA	5,179,667	Jan. 12, 1993	Iyer	—	—	
BA	5,134,699	Jul. 28, 1992	Aria et al.	—	—	
BA	5,075,886	Dec. 24, 1991	Isobe et al.	—	—	
BA	5,040,153	Aug. 13, 1991	Fung et al.	—	—	
BA	4,954,992	Sep. 4, 1990	Kumanoya et al.	—	—	
BA	4,683,555	Jul. 28, 1987	Pinkham	—	—	
BA	4,222,112	Sep. 9, 1980	Clemons et al.	—	—	
BA	4,750,839	Jun. 14, 1988	Wang et al.	—	—	
BA	5,018,109	May 21, 1991	Shinoda et al.	—	—	
BA	4,912,679	Mar. 27, 1990	Shinoda et al.	—	—	
BA	4,802,135	Jan. 31, 1989	Shinoda et al.	—	—	
BA	5,353,427	Oct. 4, 1994	Fujishima et al.	—	—	
BA	5,175,835	Dec. 29, 1992	Beighe et al.	—	—	
BA	5,210,715	May 11, 1993	Houston	—	—	
BA	5,297,091	Mar. 22, 1994	Blake et al.	—	—	
BA	5,590,081	Dec. 31, 1996	Shimizu	—	—	
BA	5,404,327	Apr. 4, 1995	Houston	—	—	
BA	4,631,659	Dec. 23, 1986	Hayn, II et al.	—	—	
BA	5,099,481	Mar. 24, 1992	Miller	—	—	

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
JA	4,646,270	Feb. 24, 1987	Voss	—	—	
MA	4,845,677	Jul. 4, 1989	Chappell et al.	—	—	
MA	4,769,778	Sep. 6, 1988	Tielert et al.	—	—	
MA	4,740,924	Apr. 26, 1988	Tielert et al.	—	—	
MA	4,866,675	Sep. 12, 1989	Kawashima	—	—	
MA	4,849,937	Jul. 18, 1989	Yoshimoto	—	—	
MA	4,712,190	Dec. 8, 1987	Gulielmi et al.	—	—	
MA	5,001,672	Mar. 19, 1991	Ebbers et al.	—	—	
MA	5,111,386	May 5, 1992	Fujishima et al.	—	—	
MA	4,928,265	May 22, 1990	Higuchi et al.	—	—	
MA	4,873,671	Oct. 10, 1989	Kowshik et al.	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
MA	0 449 052 A2	Oct 2, 1991	EPO	—	—	
MA	EP 0 218 523 B1	Jun. 19, 1996	EPO	—	—	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	H. J. Mattausch, et al., "A Memory-Based High-Speed Digital Delay Line With a Large Adjustable Length", IEEE Journal of Solid State Circuits, vol. 23, no. 1, Feb. 1988 (pp. 105-110)
MA	Iqbal, Mohammad Shakaib, "Internally Timed RAMs Build Fast Writable Control Stores," Electronic Design, pp. 93-96 (August 25, 1988)
MA	Bursky, Dave, "Advanced Self-Timed SRAM Pares Access Time to 5 ns," Electronic Design, pp. 145-147 (Feb. 22, 1990)
MA	"Bipolar/MOS Memories Data Book", Advanced Micro Devices, Sunnyvale, CA, 1986 (pp. 4-143 to 4-163)
MA	"Memories 1986-87 Databook", Fujitsu Inc., 1986 (pp. 1-102 to 1-128)
MA	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)

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<i>JA</i>	4,754,433	06/28/88	Chin et al.	—	—	
<i>JA</i>	5,023,488	06/11/91	Gunning	—	—	
<i>JA</i>	4,920,486	04/24/90	Nielson	—	—	
<i>JA</i>	4,719,602	01/12/88	Haq et al.	—	—	
<i>JA</i>	4,263,650	04/21/81	Bennet et al.	—	—	
<i>JA</i>	3,771,145	11/06/73	Wiener	—	—	
<i>JA</i>	3,691,534	09/12/72	Varadi et al.	—	—	
<i>JA</i>	3,969,706	07/13/76	Proebsting et al.	—	—	
<i>JA</i>	4,766,536	8 07/23/88	Wilson, Jr. et al.	—	—	
<i>JA</i>	4,998,262	03/05/91	Wiggers	—	—	
<i>JA</i>	4,747,079	5 03/24/88	Yamaguchi	—	—	
<i>JA</i>	4,649,511	03/10/87	Gdula	—	—	
<i>JA</i>	4,757,473	07/12/88	Kurihara et al.	—	—	

## FOREIGN PATENT DOCUMENTS

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>JA</i>	M. Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-bit Microprocessor with on-Chip Cache", IEEE Journal of Solid State Circuits, vol. 22 No. 5, pp. 790-799 (Oct. 1987)
<i>JA</i>	S. Watanabe et al., "An Experimental 16-Mbit CMOS DRAM Chip with a 100-MHz Serial READ/WRITE Mode", IEEE Journal of Solid State Circuits, vol. 24 No. 3, pp. 763-770 (June 1982)
<i>JA</i>	T.L. Jeremiah et al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul., Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982)
<i>JA</i>	L. R. Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 3, pp. 562-567 (Oct. 1983)

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<i>BA</i>	4,445,204	04/24/84	Nishiguchi	—	—	
<i>MA</i>	4,821,226	04/11/89	Christopher et al.	—	—	
<i>MA</i>	4,882,712	11/21/89	Ohno et. al.	—	—	
<i>MA</i>	4,951,251	08/21/90	Yamaguchi et al.	—	—	
<i>MA</i>	4,928,265	12/29/92	Beighe et al.	—	—	
<i>MA</i>	5,107,465	04/21/92	Fung et al.	—	—	
<i>MA</i>	5,206,833	04/27/93	Lee	—	—	
<i>MA</i>	4,953,128	08/28/90	Kawai et al.	—	—	
<i>MA</i>	5,140,688	08/18/92	White et al.	—	—	
<i>MA</i>	5,018,111	05/21/91	Madland	—	—	
<i>MA</i>	4,734,880	03/29/88	Collins	—	—	
<i>MA</i>	4,183,095	01/08/80	Ward	—	—	
<i>MA</i>	4,975,872	12/04/90	Zaiki	—	—	
<i>MA</i>	4,792,926	12/20/88	Roberts	—	—	
<i>MA</i>	4,811,202	03/07/89	Schabowski	—	—	
<i>MA</i>	4,860,198	07/22/89	Takenaka	—	—	

## FOREIGN PATENT DOCUMENTS

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	5,016,226	05/14/91	Hiwada et al.	—	—	
<i>MA</i>	5,109,498	04/28/92	Kamiya et al.	—	—	
<i>MA</i>	4,807,189	02/21/89	Pinkham et al.	—	—	
<i>MA</i>	4,092,665	05/30/78	Saran	—	—	
<i>MA</i>	4,799,199	01/17/89	Scales, III et al.	—	—	
<i>MA</i>	5,142,637	09/25/92	Harlin et al.	—	—	
<i>MA</i>	5,148,523	09/15/92	Harlin et al.	—	—	

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>MA</i>	A. Yuen et al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989)
<i>MA</i>	D.T. Wong et al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5- $\mu$ m Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988)
<i>MA</i>	T. Williams et al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988)
<i>MA</i>	D. Jones, "Synchronous static ram", Electronics and Wireless World, vol. 93, no. 1622, pp. 1243-4 (Dec. 87)
<i>MA</i>	F. Miller et al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987
<i>MA</i>	K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986)
<i>MA</i>	K. Nogami et al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990)
<i>MA</i>	F. Towler et al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989)

EXAMINER <i>John Auer</i>	DATE CONSIDERED <i>5/14/2002</i>
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MA	5,016,226	05/14/91	Hiwada et al.	—	—	
MA	4,954,987	09/04/90	Auvinen et al.	—	—	
MA	4,675,850	06/23/87	Kumanoya et al.	—	—	
MA	4,788,667	11/29/88	Nakano et al.	—	—	
MA	4,945,516	07/31/90	Kashiyama	—	—	
MA	4,937,734	06/26/90	Bechtolsheim	—	—	
MA	4,845,664	07/04/89	Aichelmann, Jr. et al.	—	—	
MA	4,920,483	04/24/90	Pogue et al.	—	—	
MA	4,680,738	07/14/87	Tam	—	—	

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference
MA	H. L. Kalter et al. "A 50-ns 16Mb DRAM with a 10-ns Data Rate and On-Chip ECC" IEEE Journal of Solid State Circuits, vol. 25 No. 5, pp. 1113-1128 (Oct 1990)
MA	D. Wendell et al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990)
MA	M. Bazes et al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983)
MA	R. Schmidt, "A memory Control Chip for Formatting Data into Blocks Suitable for Video Applications", IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1989)
MA	D. K. Morgan "The CVAX CMCTL - A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988)
MA	T.C. Poon et al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987)

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MA	4,633,735	05/05/87	Novak, et. al	—	—	
MA	5,684,753	11/04/97	Hashimoto, et al	—	—	
MA	4,322,635	03/30/81	Redwine	—	—	
MA	5,006,982	04/09/91	Ebersole et al.	—	—	
MA	4,636,986	01/13/87	Pinkham	—	—	

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	Ikkeda, Hiroaki et al., "100 MHz Serial Access Architecture for 4Md Field Memory," Symposium of VLSI Circuits, Digest of Technical Papers, pp. 11-12 (Jun. 1990)
MA	Takasugi, A. et al., "A DATA TRANSFER ARCHITECTURE FOR FAST MULTI-BIT SERIAL ACCESS MODE DRAM", 11TH European Solid State Circuits Conference, Toulouse France pp. 161-165 (Sep. 1985)
MA	Ray Pinkham et al., "A 128Kx8 70-MHz Multiport Video RAM with Auto Register Reload and 8x4 WRITE Feature," IEEE Journal of Solid State Circuits, vol. 23, no. 3, pp. 1133-1139 (Oct. 1988)
MA	Graham, Andy et al., "Pipelined static RAM endows cache memories with 1-ns speed", Electronic Design pp. 157-170 (Dec. 1984)
MA	Robert J. Lodi et al., "Chip and System Characteristics of a 2048-Bit MNOS-BORAM LSI Circuit," IEEE International Solid-State Circuits Conference, (Feb. 1976)
MA	Pinkham, Raymond, "A High Speed Dual Port Memory with Simultaneous Serial and Random Mode Access for Video Applications," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 6, pp. 999-1007 (Dec. 1984)
MA	Ishimoto, S. et al., "A 256K Dual Port Memory," ISSCC Digest of Technical Papers, p. 38-39 (Feb. 1985)

EXAMINER <i>Glen Ann</i>	DATE CONSIDERED <i>5/14/2001</i>
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MA	4,979,145	12/18/90	Remington et al.	—	—	
MA	5,276,846	01/04/94	Aichelmann Jr., et. al	—	—	
MA	4,482,999	11/13/84	Janson et al.	—	—	
MA	5,193,193	03/09/93	Iyer	—	—	
MA	4,926,385	05/15/90	Fujishima et al.	—	—	
MA	4,566,099	01/21/86	Magerl	—	—	
MA	4,803,621	02/07/89	Kelly	—	—	
MA	4,589,108	05/13/86	Billy	—	—	
MA	4,870,622	09/26/89	Aria et al.	—	—	
MA	4,878,166	10/31/89	Johnson et al.	—	—	
MA	4,849,965	07/18/89	Chomel et al.	—	—	
MA	4,851,990	07/25/89	Johnson et al.	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
MA	Sho 62-71428	10/05/88	JP	—	—	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	Tomoji Takada et al., "A Video Codec LSI for High-Definition TV Systems with One-Transistor DRAM Line Memories," IEEE Journal of Solid-State Circuits, Vol. 24, No. 6, pp. 1656-1659 (Dec. 1989)
MA	Amitai, Z., "Burst Mode Memories Improve Cache Design," WESCON/90 Conference Record, pp. 29-32 (Nov. 1990)
MA	Robert J. Lodi et al., "MNOS-BORAM Memory Characteristics," IEEE Journal of Solid-State Circuits, vol. SC-11, No. 5, pp. 622-631 (Oct. 1976)

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<i>MA</i>	4,048,673	09/13/77	Hendrie et al.	—	—	
<i>MA</i>	4,519,034	05/21/85	Smith et al.	—	—	
<i>MA</i>	4,748,617	05/31/88	Drewlo	—	—	
<i>MA</i>	4,839,801	06/13/89	Nicely et al.	—	—	
<i>MA</i>	4,949,301	08/14/90	Joshi et al.	—	—	
<i>MA</i>	3,950,735	04/13/76	Patel	—	—	
<i>MA</i>	4,047,246	09/06/77	Kerilenevich et al.	—	—	
<i>MA</i>	5,029,124	07/02/91	Leahy et al.	—	—	
<i>MA</i>	4,763,249	08/09/88	Bomba et al.	—	—	
<i>MA</i>	4,625,307	11/25/86	Tulpule et al.	—	—	

## FOREIGN PATENT DOCUMENTS

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<i>MA</i>	S63-142445	June 14, 1988	Japan	—	—	
<i>MA</i>	B63-46864	Sept. 19, 1988	Japan	—	—	
<i>MA</i>	S64-29951	Jan. 31, 1989	Japan	—	—	
<i>MA</i>	S61-72350	April 14, 1986	Japan	—	—	
				—	—	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>MA</i>	E.H. Frank "The SBUS: Sun's High Performance System Bus for RISC Workstations" Sun Microsystems Inc. 1990
<i>MA</i>	K. Numata et. al. "New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989)

EXAMINER <i>Glean Anne</i>	DATE CONSIDERED <i>5/14/2002</i>
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	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE December 21, 2001	GROUP ART UNIT 2181

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	4,330,852	May 18, 1982	Redwine et al.	—	—	
<i>MA</i>	4,703,418	Oct. 27, 1987	James	—	—	
<i>MA</i>	4,785,394	Nov. 15, 1987	Fischer	—	—	
<i>MA</i>	4,726,021	Feb. 16, 1988	Horiguchi et al.	—	—	
<i>MA</i>	4,870,562	Sept. 26, 1989	Kimoto et al.	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>MA</i>	S56-82961	July 7, 1981	Japan	—	—	
<i>MA</i>	S57-14922	Jan. 26, 1982	Japan	—	—	
<i>MA</i>	Sho 60-80193	May 8, 1983	Japan	—	—	
<i>MA</i>	Sho 60-55459	Mar. 30, 1985	Japan	—	—	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>MA</i>	European Search Report for EPO Patent Application No. 00 101 1832
<i>MA</i>	European Search Report for EPO Patent Application No. 89 30 2613
<i>MA</i>	Z. Amitai, "New System Architectures for DRAM Control and Error Correction", Monolithic Memories Inc., Electro/87 and Mini/Mico Northeast: Focusing on the OEM Conference Record, pp. 1132, 4/31-3, (April 1987)
<i>MA</i>	N. Siddique, "100-MHz DRAM Controller Sparks Multiprocessor Designs", Electronic Design, pp. 138-141, (Sept 1986)
<i>MA</i>	H. Kuriyama et al., "A 4-Mbit CMOS SRAM WITH 8-NS SERIAL ACCESS TIME", IEEE Symposium On VLSI Circuits Digest Of Technical Papers, pp. 51-52, (June 1990)
<i>MA</i>	J. Chun et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 83-86, (Nov. 1988)
<i>MA</i>	A. Fielder et al., "A 3 NS 1K X 4 STATIC SELF-TIMED GaAs RAM", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pp. 67-70, (Nov. 1988)
<i>MA</i>	JEDEC Standard No. 21C
<i>MA</i>	European Search Report for EPO Patent Application No. 00 10 0018
<i>MA</i>	European Search Report for EPO Patent Application No. 00 10 822

EXAMINER <i>Glenn June</i>	DATE CONSIDERED <i>5/14/2002</i>
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	FILING DATE December 21, 2001	GROUP ART UNIT 2181

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
DA	4,205,373	May 27, 1980	Shah et al.	—	—	
DA	4,845,670	Jul. 4, 1989	Nishimoto et al.	—	—	
DA	4,509,142	Apr. 2, 1985	Childers	—	—	
DA	4,183,095	Jan. 8, 1980	Ward	—	—	
DA	4,685,088	Aug. 4, 1987	Ianucci	—	—	
DA	5,390,149	02/14/95	Vogley et al.	—	—	
DA	4,570,220	02/11/86	Tetrick et al.	—	—	
DA	5,083,296	01/21/92	Hara et al.	—	—	
DA	5,077,693	12/31/91	Hardec et al.	—	—	
DA	4,916,670	04/10/90	Suzuki et al.	—	—	
DA	4,247,817	1/27/81	Heller	—	—	
DA	5,301,278	04/05/94	Bowater et al.	—	—	
DA	4,970,418	11/13/90	Masterson	—	—	
DA	5,361,277	11/01/94	Grover	—	—	
DA	4,519,034	05/21/85	Smith et al.	—	—	
DA	4,315,308	02/09/82	Jackson	—	—	
DA	3,821,715	06/28/74	Hoff, Jr et al.	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
DA	0 246 767	April 28, 1987	EPO	—	—	
DA	0 334 552	Mar. 16, 1989	EPO	—	—	
DA	0 276 871	Jan. 29, 1988	EPO	—	—	

EXAMINER <i>Glenn Ann</i>	DATE CONSIDERED <i>5/14/2002</i>
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## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	5,034,964	Jul.23, 1991	Khan et al	—	—	
<i>MA</i>	4,630,193	Dec. 16, 1986	Kris	—	—	
<i>MA</i>	4,710,904	Dec. 1, 1987	Suzuki	—	—	
<i>MA</i>	4,739,502	Apr. 19, 1988	Nozaki	—	—	
<i>MA</i>	4,905,201	Feb. 27, 1990	Ohira et al.	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>MA</i>	SHO 58-192154	Nov. 9, 1983	Japan	—	—	
<i>MA</i>	SHO 63-34795	Feb. 15, 1988	Japan	—	—	
<i>MA</i>	SHO 61-107453	May 26, 1986	Japan	—	—	
<i>MA</i>	SHO 63-91766	April 22, 1988	Japan	—	—	
<i>MA</i>	SHO 62-16289	Jan. 24, 1987	Japan	—	—	
<i>MA</i>	SHO 61-160556	Oct. 4, 1986	Japan	—	—	

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>MA</i>	Watanabe, T.; "Session XIX: High Density SRAMS"; IEEE International Solid State Circuits Conference pp. 266-267 (1987)
<i>MA</i>	Ohno, C.; "Self-Timed RAM: STRAM"; Fujitsu Sci. TechJ., 24, 4, pp 293-300 (Dec. 1988)
<i>MA</i>	"Fast Packet Bus for Microprocessor Systems with Caches", IBM Technical Disclosure Bulletin, pp.279-282 (Jan 1989)
<i>MA</i>	Gustavson, D. "Scalable Coherent Interface"; Invited Paper, COMPCON Spring '89, San Francisco, CA; IEEE, pp. 536-538 (Feb 27-Mar 3, 1989)
<i>MA</i>	James, D.; "Scalable I/O Architecture for Busses"; IEEE, pp. 539-544 (April 1989)

EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>5/14/2002</i>
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## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
MA	4,755,937	July 5, 1989	Glier	—	—	

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATED YEARS

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MA	Grover et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", IEEE Paper 47.2 Globecom, 1988, pp 1544-1548
MA	Knut Alnes, "Scalable Coherent Interface", SCI-Feb89-doc52, (To appear in Eurobus Conference Proceedings May 1989), pp. 1-8.
MA	Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, August 22, 1988
MA	Moussouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5))
MA	Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148
MA	Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130
MA	"LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15
MA	"LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp 1-20
MA	"High Speed CMOS Databook", Integrated Device Technology Inc. Santa Clara, CA, 1988 pp 9-1 to 9-9
MA	"IDT 79R2010 RISC Floating Point Accelerator (FPA) Advance Information", Integrated Device Technology Inc. Santa Clara, CA, 1987, pp. 9-10 to 9-14
MA	Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83

EXAMINER <i>Glover Anne</i>	DATE CONSIDERED <i>5/14/2002</i>
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